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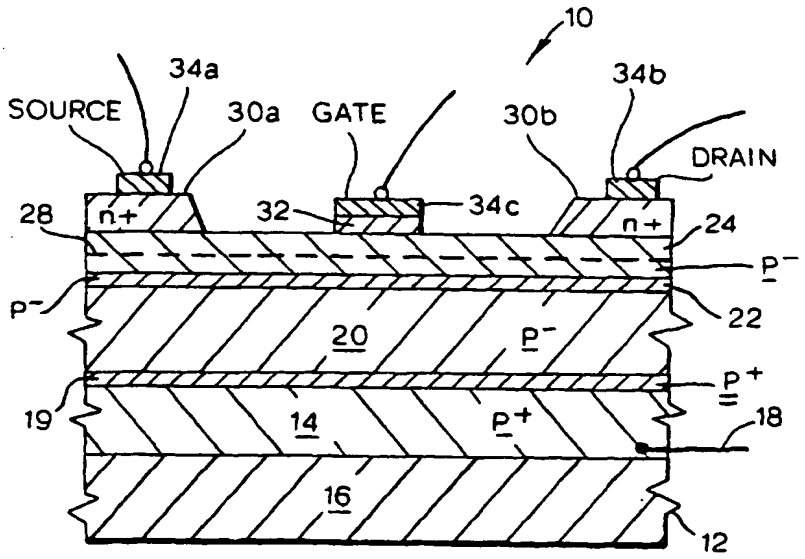
(54) Title: CHARGE CARRIER EXTRACTING TRANSISTOR




(57) Abstract: An extracting transistor (10) - an FET - includes a conducting channel extending via a p-type InSb quantum well (22) between p-type InA1Sb layers (20, 24) of wider band-gap. One of the InA1Sb layers (24) incorporates an ultra-thin n-type δ-doping layer (28) of Si, which provides a dominant source of charge carriers for the quantum well (22). It bears $n^+$ source and drain electrodes (30a, 30b) and an insulated gate (30c). The other InA1Sb layer (20) adjoins a barrier layer (19) of still wider band-gap upon a substrate layer (14) and substrate (16) with electrode (18). Biasing one or both of the source and drain electrodes (30a, 30b) positive relative to the substrate electrode (18) produces minority carrier extraction in the quantum well (22) reducing its intrinsic contribution to conductivity, taking it into an extrinsic saturated regime and reducing leakage current.

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# CHARGE CARRIER EXTRACTING TRANSISTOR

This invention relates to an extracting transistor, that is to say a transistor in which intrinsic conductivity is reduced by carrier extraction.

Before considering the prior art, semiconductor nomenclature and properties will be discussed. Transistor operation relies on electrical transport effects in semiconductor material, and, broadly speaking, there are three important conduction regimes: unsaturated extrinsic, saturated extrinsic and intrinsic, and these occur at low, intermediate and high temperature respectively. In the unsaturated extrinsic regime, there is insufficient thermal energy to ionise all impurities and the carrier concentration is temperature dependent because more impurities are ionised as temperature increases. Carriers are thermally activated from dopant impurities of a single species, i.e. donors or acceptors. Conduction is due substantially to one kind of carrier in one band, i.e. electrons in the conduction band or holes in the valence band but not both. The saturated extrinsic regime is similar, but occurs at higher temperatures at which virtually all impurities have become ionised but insufficient thermal energy is available to ionise significant numbers of valence band states to create electron-hole pairs: here the carrier concentration is largely independent of temperature.

In the intrinsic regime, conduction has a substantial contribution from thermal ionisation of valence band states producing both types of carrier, i.e. electron-hole pairs, in addition to carriers of one type activated from impurities. Conduction is due to both kinds of carrier in both bands, i.e. electrons in the conduction band and holes in the valence band. Conductivity varies with temperature in this regime because the electron-hole pair concentration is temperature dependent. There is an intervening transition region between the extrinsic and intrinsic regimes where conduction is partially extrinsic and partially intrinsic giving rise to more of one type of charge carrier than the other, i.e. majority carriers and minority carriers: it is at or near ambient temperature in Ge depending on doping. The onset temperature of intrinsic conduction depends on band

gap and dopant concentration; it can occur below ambient temperature, as low as 150K in narrow gap semiconductors with low doping.

Materials such as Si and GaAs with a saturated extrinsic regime at ambient temperature are preferred for transistor applications despite their inferior mobility properties: this is because of the need for very low intrinsic carrier concentrations in the active regions of devices. Highly pure Ge is intrinsic at ambient temperature, and by analogy with this weakly doped Si is sometimes referred to wrongly as intrinsic, such as in PIN diodes where the high resistivity I ("intrinsic") region is in fact extrinsic at ambient temperature. The purest Si currently available is more than an order of magnitude too impure to be intrinsic at ambient temperature.

Narrow band-gap semiconductors such as indium antimonide (InSb) have useful properties such as very low electron effective mass, very high electron mobility and high saturation velocity. These are potentially of great interest for ultra high speed transistor applications. InSb in particular is a promising material for fast, very low power dissipation transistors, because its electron mobility $\mu_e$ at low electric fields is nine times higher than that of GaAs and its saturation velocity $v_{sat}$ is more than five times higher, despite GaAs having better properties than Si in these respects. InSb is also predicted to have a large ballistic mean free path of over 0.5 μm. This suggests that InSb has potential for high speed operation at very low voltages with consequent low power consumption, which would make it ideal for portable and high-density applications. Some of the properties of Silicon, GaAs and InSb at 295K (ambient temperature) are compared in Table 1 below.

Table 1: Properties of InSb at 295 K

| Parameter | Silicon | GaAs | InSb | Units |
|---|---|---|---|---|
| $E_G$ Band-gap | 1.12 | 1.43 | 0.175 | eV |
| $m^*_e$ Electron Effective Mass | 0.19 | 0.072 | 0.013 | $m_0$ |
| $\mu_e$ Electron Mobility | 1,500 | 8,500 | 78,000 | $cm^2 V^{-1} s^{-1}$ |
| $v_{sat}$ Saturation Velocity | $1'10^7$ | $1'10^7$ | $>5'10^7$ | $cm\ s^{-1}$ |
| $l_e$ Electron Mean Free Path | 0.04 | 0.15 | 0.58 | μm |
| $n_i$ Intrinsic Carrier Concentration | $1.6'10^{10}$ | $1.1'10^7$ | $1.9'10^{16}$ | $cm^{-3}$ |

Until recently, the potentially valuable properties of InSb have been inaccessible at ambient temperatures due to its low band-gap and consequently high intrinsic carrier concentration (~$2x10^{16}$ $cm^{-3}$), which is six and nine orders of magnitude above those of Si and GaAs respectively. This leads to InSb devices exhibiting high leakage currents at normal operating temperatures at or near ambient temperature of 295K, where the minority carrier concentration is much greater than the required value at normal doping levels. It was thought for many years that this was a fundamental problem which debarred InSb and other narrow band-gap materials from use in devices at ambient temperature and above.

The problem was however overcome to some extent in the invention the subject of US Pat. No. 5,382,814: this patent discloses a non-equilibrium metal-insulator-semiconductor field effect transistor (MISFET) using the phenomena of carrier exclusion and extraction to reduce the intrinsic contribution to the carrier concentration below the equilibrium level. The MISFET is a reverse-biased $p^+\underline{p}^+p^-n^+$ structure, where p denotes an InSb layer, $\underline{p}$ is a strained $In_{1-x}Al_xSb$ layer (underlined $\underline{p}$ indicates

wider band-gap than p), $p^-$ indicates a weakly doped p-type region that is intrinsic at ambient operating temperature, and the + superscript indicates a high dopant concentration; these four layers define three junctions between adjacent layer pairs, i.e. $p^+p^+$, $p^+p^-$ and $p^-n^+$ junctions respectively. The active region of the device is the $p^-$ region, and minority carriers are removed from it at the $p^-n^+$ junction acting as an extracting contact. The $p^+p^-$ junction is an excluding contact which inhibits re-introduction of these carriers. In consequence, under applied bias the minority carrier concentration falls in the active region, and the majority carrier concentration falls with it to a like extent to preserve charge neutrality. This reduces electron and hole concentrations by like amounts, which corresponds to a reduction in the intrinsic contribution to conductivity (electron-hole pairs) and takes the active region into an extrinsic-like regime.

International Patent Application No. WO 99/28975 published under the Patent Cooperation Treaty relates to a similar transistor which has a straightened channel to improve frequency response. These prior art extracting devices however suffer from the problem that they exhibit relatively high leakage current which increases power requirements and operating temperature.

It is an object of the invention to provide an alternative form of extracting transistor capable of operation with lower leakage current than the prior art.

An extracting transistor characterised in that:

a) it is a field effect transistor incorporating a conducting region consisting at least partly of a quantum well;

b) the quantum well is in an at least partially intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and

c) it includes at least one junction which is biasable to reduce intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

The invention provides the advantage that with transistor design in accordance with ordinary skill in the art of semiconductor device fabrication it is capable of reducing leakage current considerably: examples of the invention have exhibited an order of magnitude reduction in leakage current.

The transistor of the invention may contain an excluding junction for inhibiting minority carrier supply to the quantum well; it may be arranged for carrier exclusion at least partly by incorporation of an excluding heterojunction between two semiconductor materials of differing band-gap both wider than that of the quantum well.

The biasable junction may be an extracting junction for removal of carriers from the quantum well. It may be a heterojunction between indium antimonide and a semiconductor material having a wider band gap than indium antimonide: e.g. indium aluminium antimonide with x is in the range 0.10 to 0.5, preferably 0.15 to 0.2 or substantially 0.15.

The excluding junction may be a heterojunction between indium antimonide and a semiconductor material having a wider band gap than indium antimonide.

The quantum well material may have a band gap less than 0.4 eV, and may be indium antimonide.

In a preferred embodiment, the transistor of the invention includes a δ-doping layer arranged to be a dominant source of charge carriers for the quantum well. It may have an $n^+$-$p^-$ - quantum well - $p^-$-$p^+$-$p^+$ diode structure or an $n^+$-$p^-$ - quantum well - $p^-$-$p^+$ diode structure.

The transistor of the invention may include a first excluding junction for inhibiting minority carrier supply to the quantum well and wide band-gap barrier layer to enhance

such inhibiting effect. It may include a gate contact insulated from the active region by insulating material such as silicon dioxide or wide band-gap semiconductor material.

The transistor may alternatively include a gate contact deposited directly upon a surface of the active region and forming a Schottky contact thereto.

In one embodiment, the transistor includes source, gate and drain electrodes and a substrate contact, the biasable junction is a pn junction reverse biasable via the substrate contact to produce minority carrier extraction from the quantum well, and the substrate contact is connected externally to the source electrode.

The transistor may be p-channel with a $p^+$-$\underline{n}^-$-quantum well - $\underline{n}^-$-$\underline{\underline{n}}^+$-$\underline{n}^+$ or a $p^+$-$\underline{p}^-$-quantum well - $\underline{p}^-$-$\underline{\underline{n}}^+$-$n^+$ structure, and include a δ-doping layer providing a predominant source of holes for the active region.

In another aspect, the invention provides a method of obtaining transistor operation characterised in that it includes the steps of:

a) providing an extracting field effect transistor incorporating:

i) source, gate and drain electrodes and a substrate contact and between such electrodes and contact a pn junction biasable via the substrate contact for minority carrier extraction;

ii) a conducting region consisting at least partly of a quantum well in an at least partially intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and

iii) at least one junction which is biasable to reduce intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime;

b) biasing the substrate contact to reverse bias the pn junction and to arrange for the substrate contact either to be at the same potential as the source electrode, or to be negative or positive with respect to the source

electrode according to whether such electrode is associated with a p-type or n-type component of the pn junction.

In order that the invention might be more fully understood, an embodiment thereof will now be described, by way of example only, with reference to the accompanying single figure drawing, which is a schematic vertical sectional view of an extracting transistor of the invention.

Referring to the drawing, an extracting, depletion mode, field effect transistor (FET) 10 is shown, but as indicated by zigzag lines such as 12 it is not drawn to scale. The FET 10 incorporates a 1 μm thick substrate layer 14 of $p^+$-type $In_{0.85}Al_{0.15}Sb$ with a high dopant concentration of $2x10^{18}.cm^{-3}$ upon an insulating substrate 16 of GaAs and having an electrical bias contact 18, which optionally may be relocated more remotely. The layer 14 bears an optional 20 nm thick barrier layer 19 of $\underline{p}^+$-type $In_{0.7}Al_{0.3}Sb$ with a high dopant concentration $2x10^{18}$ $cm^{-3}$: here double underlining of $\underline{p}^+$ indicates wider band-gap than $p^+$, which in turn (as has been said) indicates wider band-gap than p. The barrier layer 19 is surmounted by an 0.5 μm thick layer 20 of $p^-$-type $In_{0.85}Al_{0.15}Sb$ which is doped at less than $3x10^{16}$ $cm^{-3}$.

Upon the layer 20 there is a 15 nm thick quantum well 22 of $p^-$-type InSb with a dopant concentration of less than $3x10^{16}$ $cm^{-3}$. The quantum well 22 is in turn surmounted by a 150 nm thick layer 24 (acceptable thickness range 100-200 nm): the latter consists largely of less than $3x10^{16}$ $cm^{-3}$ $p^-$-type $In_{0.85}Al_{0.15}Sb$; it incorporates an ultra-thin silicon n-type δ-doping layer 28. The δ-doping layer 28 is indicated by a chain line and is spaced apart from the quantum well 22 by a distance in the range 10-40 nm. It provides a two-dimensional electron gas with concentration per unit area in the range $6x10^{11}$ $cm^{-2}$ to $2x10^{12}$ $cm^{-2}$, e.g. $1x10^{12}$ $cm^{-2}$: the gas forms in the quantum well 22 because it is energetically favourable - this is referred to as modulation doping, and the electron gas concentration remains substantially independent of temperature because it is a function of dopant concentration only.

The layer 24 has deposited upon it two outer n+ contact regions 30a and 30b of InSb 30 nm thick and a central insulator layer 32, and the latter 30a, 30b and 32 are in turn surmounted. by respective metal layers 34a, 34b and 34c (collectively 34). The insulator layer 32 may be silicon dioxide or a semiconductor material of wider band-gap than that of InSb. The metal layers 34 are electrical connections and act respectively as FET source and drain electrodes for the FET 10. The n+ contact regions 30a and 30b are separated by a distance in the range 0.5 to 2 μm, e.g. 1 μm.

The FET 10 is an $n^+$-$p^-$-quantum well - $p^-$-$p^+$-$p^+$ diode structure in which the quantum well 22 undergoes carrier extraction when a reverse bias is applied, i.e. with one or both of the source and drain electrodes 34a and 34b biased positive with respect to the substrate layer contact 18. This is because the interfaces between layer 24 and each of layers 30a/30b is an $n^+p^-$ junction which is an extracting contact when reverse biased. The carrier concentration in the quantum well 22 is reduced by bias to considerably below the intrinsic equivalent which prevails in the absence of bias, and here again it becomes largely independent of temperature simulating a saturated extrinsic regime: this provides a low leakage current between source 34a and drain 34b when negative bias is applied to the gate 34c to turn off the FET 10. Electrons from the δ-doping layer 28 are then the dominant source of charge carriers in the quantum well 22. The FET active region, i.e. the gate-controlled conducting channel between contact layers 30a and 30b is largely that in the quantum well 22. Layers 14, 19, 20 and 24 of the FET 10 have much wider band-gap than the quantum well 22 and the leakage current contributions from these regions can be ignored.

The principle of carrier extraction is known in the prior art and is described in for example European Patent No EP 0167305 and US Patent No 5,016,073. It involves removing minority carriers from a semiconductor region at a greater rate than they are replaced; it occurs at a biased pn junction 24/30 to which minority carriers diffuse and over which they are swept by its potential drop - i.e. at which they are extracted and become lost to the region. These carriers (electrons in this case) cannot be replenished in the quantum well 22 because the only available source is the $p^-$ layer 20 which has

an inadequate (negligible) concentration of them: i.e. the $p^-p^-$ junction between layers 20 and 22 and the $p^+p^-$ junction between layers 19 and 20 are what is referred to as excluding contacts which inhibit minority carriers reaching the quantum well 22.

In the FET 10 the carrier concentration in the quantum well (22) is kept low and temperature independent: this makes it more suitable than prior art devices for demanding applications. It performs well in this regard because the quantum well carrier concentration is very largely determined by modulation doping, which is a temperature-independent parameter unlike thermal activation of electron-hole pairs. The FET's off-state drain leakage current under bias (i.e. source-drain current with gate biased to cut-off) is at least an order of magnitude lower than comparable prior art devices.

By virtue of the gate insulation layer 32, the FET 10 is a metal-insulator-semiconductor device, i.e. a MISFET. It is possible to dispense with the insulation layer 32, which would make the gate electrode 34c a Schottky contact to the $p^-$ layer 24. In this Schottky case the FET transconductance is about 3-4 times higher than that of a comparable prior art device with a typical gate oxide thickness of around 30 – 70 nm. Output conductance is typically half that of comparable prior art devices the subject of US Pat. No. 5,382,814 and International Patent Application No. WO 99/28975 published under the Patent Cooperation Treaty. These properties are obtained largely as a result of the preponderance of wide band-gap semiconductor material in the FET 10: such material gives low leakage current and confinement of carriers in the quantum well 22 providing good transistor action i.e. high gain and low output conductance.

The barrier layer 19 is also optional because the FET 10 is viable without it: it is intended to provide lower off-state leakage current by providing more efficient carrier exclusion, but it is not known how significant this effect is. It provides an excluding junction between layers 19 and 20 additional to that between layers 20 and 22: this additional junction is a heterojunction between two semiconductor materials of like

conductivity type (p-type) but differing band-gap both larger than that of indium antimonide.

The FET 10 may be operated with the substrate layer contact 18 reverse biased with respect to the source electrode 34a, or with the contact 18 and electrode 34a at the same potential, or with these shorted together. Since the FET 10 is largely p-type with n-type layers 30a and 30b, a reverse biased substrate layer contact 18 is negatively biased with respect to the source electrode 34a; for an equivalent FET of reversed layer conductivity type, i.e. p-type contact layers equivalent to layers 30a and 30b and other layers n-type, a reverse biased substrate layer contact 18 would be positively biased with respect to a source electrode; i.e. the substrate layer contact 18 is positive or negative with respect to the source electrode (34a) according to whether such electrode is associated with a n-type or p-type component (30a) of the extracting pn junction (24/30).

The FET 10 is an n-channel device because electrons provide conduction in the quantum well 22. A p-channel equivalent is formed by changing each layer 14/19/20/22/24/30 in the FET 10 to its respective opposite conductivity type: i.e. the $n^+$-$p^-$-quantum well - $\underline{p}^-$-$\underline{p}^+$-$\underline{p}^+$ structure becomes a $p^+$-$\underline{n}^-$-quantum well - $\underline{\underline{n}}^-$-$\underline{\underline{n}}^+$-$\underline{n}^+$ structure with a δ-doping layer of berylllium providing a predominant source of holes for the quantum well equivalent of layer 22. It is not in fact essential to change the conductivity types of the equivalents of the quantum well and its adjacent layers, i.e. layers 22, 20 and 24: these have low dopant concentrations and therefore do not greatly affect device operation; if they are not changed the resulting structure is $p^+$-$p^-$-quantum well - $p^-$-$\underline{\underline{n}}^+$-$n^+$. Either of these p-channel devices may be advantageous because each contains a strained quantum well equivalent to layer 22, and such a well is believed to raise hole mobility due to more light hole transport.

## CLAIMS

1. An extracting transistor characterised in that:

a) it is a field effect transistor (10) incorporating a conducting region (20, 22, 24) consisting at least partly of a quantum well (22);

b) the quantum well (22) is in an at least partially intrinsic conduction regime when the transistor (10) is unbiased and at a normal operating temperature; and

c) it includes at least one junction (24/30) which is biasable to reduce intrinsic conduction in the quantum well (22) and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

2. A transistor according to Claim 1 characterised in that it contains an excluding junction (20/22) for inhibiting minority carrier supply to the quantum well (22).

3. A transistor according to Claim 1 or 2 characterised in that it is arranged for carrier exclusion at least partly by incorporation of an excluding heterojunction (19/20) between two semiconductor materials of differing band-gap both wider than that of the quantum well (22).

4. A transistor according to Claim 1 characterised in that the biasable junction is an extracting junction (24/30a, 24/30b) for removal of carriers from the quantum well (22).

5. A transistor according to Claim 4 characterised in that the extracting junction (24/30) is a heterojunction between indium antimonide (30) and a semiconductor material (24) having a wider band gap than indium antimonide.

6. A transistor according to Claim 5 characterised in that the wider band gap material (24) is an indium aluminium antimonide material.

7. A transistor according to Claim 6 characterised in that the indium aluminium antimonide material is $In_{1-x}Al_xSb$ where x is in the range 0.10 to 0.5.

8. A transistor according to Claim 7 characterised in that x is in the range 0.15 to 0.2.

9. A transistor according to Claim 8 characterised in that x is substantially 0.15.

10. A transistor according to Claim 1 characterised in that the quantum well (22) material has a band gap less than 0.4 eV.

11. A transistor according to Claim 1 characterised in that the quantum well (22) is of indium antimonide material.

12. A transistor according to any preceding claim characterised in that it includes a δ-doping layer arranged to be a dominant source of charge carriers for the quantum well (22).

13. A transistor according to any preceding claim characterised in that it has an $n^+$-$\underline{p}^-$ - quantum well - $\underline{p}^-$-$\underline{p}^+$-$\underline{p}^+$ diode structure.

14. A transistor according to any preceding claim characterised in that it has an $n^+$-$\underline{p}^-$ - quantum well - $\underline{p}^-$-$\underline{p}^+$ diode structure.

15. A transistor according to Claim 1 characterised in that it includes a first excluding junction (20/22) for inhibiting minority carrier supply to the quantum well (22) and a wide band-gap barrier layer (19) to enhance such inhibiting effect

16. A transistor according to any preceding claim characterised in that it includes a gate contact (34c) insulated from the active region (24) by insulating material (32).

17. A transistor according to Claim 16 where the insulating material (32) is silicon dioxide.

18. A transistor according to any one of Claims 1 to 15 characterised in that it includes a gate contact (34c) separated from the active region (22, 24) by semiconductor material (32) of wider band-gap than that of region 24.

19. A transistor according to any one of Claims 1 to 15 characterised in that it includes a gate contact deposited directly upon a surface of the active region (22, 24) and forming a Schottky contact thereto.

20. A transistor according to Claim 1 characterised in that it includes source, gate and drain electrodes (34) and a substrate contact (18), the biasable junction is a pn junction (24/30) reverse biasable via the substrate contact (18) to produce minority carrier extraction from the quantum well (22), and the substrate contact (18) is connected to the source electrode (34a).

21. A transistor according to Claim 1 characterised in that it is a p-channel transistor.

22. A transistor according to Claim 21 characterised in that it is a $p^+$-$\underline{n}^-$-quantum well - $\underline{n}^-$-$\underline{\underline{n}}^+$-$\underline{n}^+$ structure with a δ-doping layer providing a predominant source of holes for the active region.

23. A transistor according to Claim 21 characterised in that it is a $p^+$-$\underline{p}^-$-quantum well - $\underline{p}^-$-$\underline{\underline{n}}^+$-$n^+$ structure with a δ-doping layer providing a predominant source of holes for the active region.

24. A method of obtaining transistor operation characterised in that it includes the steps of:

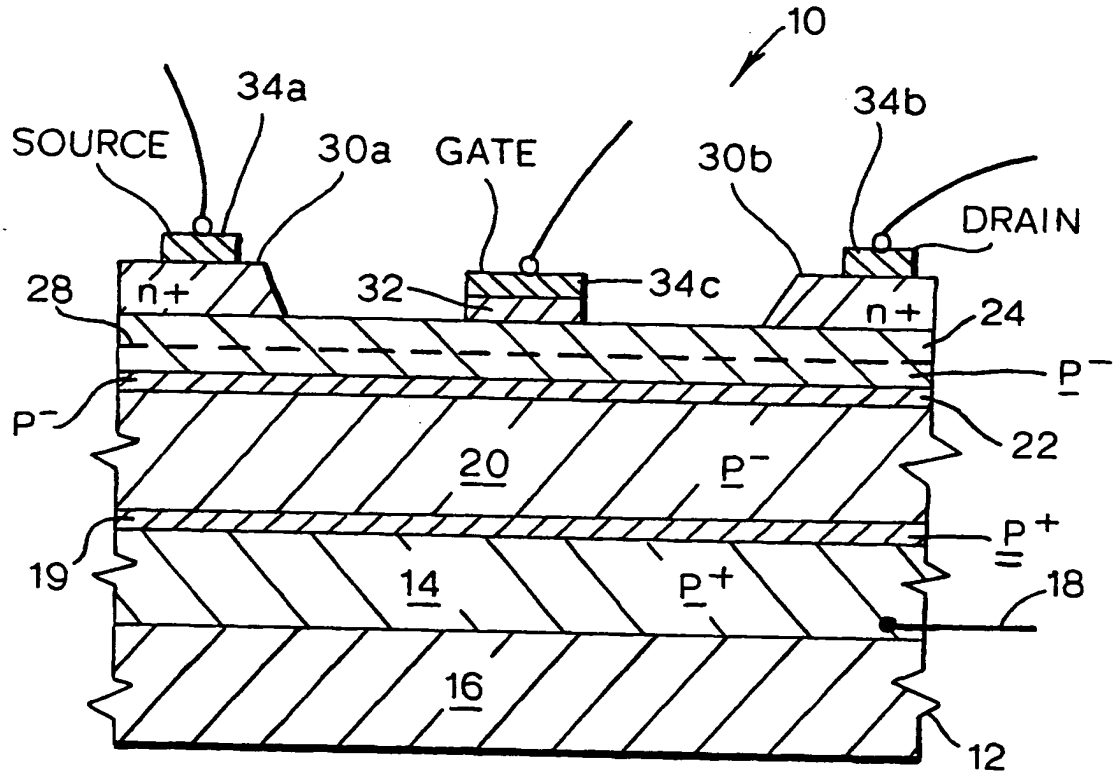
a) providing an extracting field effect transistor (10) incorporating

i) source, gate and drain electrodes (34) and a substrate contact (18) and between such electrodes and contact a pn junction (24/30) biasable via the substrate contact (18) for minority carrier extraction;

ii) a conducting region (20, 22, 24) consisting at least partly of a quantum well (22) in an at least partially intrinsic conduction regime when the transistor (10) is unbiased and at a normal operating temperature; and

iii) at least one junction (24/30) which is biasable to reduce intrinsic conduction in the quantum well (22) and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime;

b) biasing the substrate contact (18) to reverse bias the pn junction (24/30) and to arrange for the substrate contact (18) either to be at the same potential as the source electrode (34a), or to be positive or negative with respect to the source electrode (34a) according to whether such electrode is associated with a n-type or p-type component (30a) of the pn junction (24/30).



# INTERNATIONAL SEARCH REPORT

national Application No
T/GB 01/01919

A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

*Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched*

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| Y | GB 2 331 841 A (SECR DEFENCE)<br>2 June 1999 (1999-06-02)<br>page 1<br>page 13, line 14 - line 19; figures 3,5<br>page 8, line 1 -page 1, line 2; figure 1<br>page 17, line 11 -page 18, last line<br>page 20, line 1 - line 6<br>---<br>-/-- | 1-24 |

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PCT/GB 01/01919

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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